What is claimed is:

1. A method for forming an adjacent symbol codeword comprising:

generating a set of m bits, wherein m is an integer, of a first symbol and a set of m bits of a second symbol from a first set of data during a first clock phase; and

generating a set of n bits, wherein n is an integer, of the first symbol and a set of n bits of the second symbol from a second set of data during a second clock phase.

2. The method of claim 1 wherein the first and second set of data is from a memory.

3. The method of claim 2 wherein the memory is a Double Data Rate (DDR) memory.

4. The method of claim 1 wherein both m and n are four bits and constitute a nibble.

5. The method of claim 1 wherein the adjacent symbol codeword comprises an adjacent formation of the first and second symbol.

6. The method of claim 1 further comprising isolating a common mode error across the m and n bits of the first and second symbol.

7. A method for testing a memory comprising:

generating a plurality of check bits to append to data that is forwarded to the memory;

generating an adjacent symbol codeword based at least in part on data received from the memory;

decoding the adjacent symbol codeword; and

determining whether an error exists in the memory

8. The method of claim 7 wherein decoding the adjacent symbol codeword comprises generating a syndrome based at least in part on the adjacent symbol codeword.

9. The method of claim 7 wherein determining whether an error exists in the memory is based at least in part on the syndrome.

10. The method of claim 9 wherein an error exists based on the syndrome, further comprising:

classifying the error in the received data; and

correcting the error in the received data.

11. The method of claim 7 wherein the memory is a Double Data Rate (DDR) memory.

12. The method of claim wherein the syndrome is thirty two bits based on a two hundred eighty eight bit codeword.

13. An apparatus for an Error Correcting Code comprising:

a first logic to generate a plurality of check bits based on a set of data, to append the check bits to the set of data that is to be forwarded to a memory;

a second logic to receive a codeword from the memory and to generate a syndrome based on the codeword, and to detect whether an error exists based on the syndrome;

a third logic to classify the error if it exists; and

a fourth logic to correct the error if it exists.

14. The apparatus of claim 13 is incorporated within a server chipset.

15. The apparatus of claim 13 wherein the memory is a Double Data Rate (DDR) memory.

16. The apparatus of claim 13 wherein the syndrome is thirty two bits and the codeword is 288 bits.

17. The apparatus of claim 13 wherein the first logic is an encoder and utilizes the formula:

$c_i = \Sigma\, d_j \times G_{ij}$ for i=0 to 31 and j= 0 to 255,

to generate the plurality of check bits.

18. The apparatus of claim 13 wherein the second logic is a decoder and the syndrome is an H matrix that is generated by the formula:

$s_{i=} \Sigma v_j \times H_{ij}$ for i=0 to 31 and j= 0 to 287,

to generate the syndrome.

19. An apparatus to classify an error from a memory comprising:

a first logic to generate an H matrix syndrome; and

to determine whether an error exists based on the syndrome, if so, to classify an error type of the error.

20. The apparatus of claim 19, wherein the H matrix syndrome is generated by the formula:

$s_{i=} \Sigma v_j \times H_{ij}$ for i=0 to 31 and j= 0 to 287.

21. The apparatus of claim 19 wherein to classify the error type comprises the first logic to generate an error location vector.

22. The apparatus of claim 21 wherein the error location vector determines whether the error is correctable:

a value of zero in the error location vector indicates the error is uncorrectable; in contrast, a value that is greater than zero in an indicated column of the error location vector indicates the error is correctable.

23. The apparatus of claim 19 wherein the error type may be either a single device error or a double device error.

24. The apparatus of claim 23 wherein the double device error is either of a simultaneous error or a sequential error.

25. The apparatus of claim 23 wherein the single device error is classified based on a weight of an error value, e_o and e_1, and the error location vector is to gate the error values.

26. A system comprising:

a processor, coupled to a memory and a chipset, to generate an operation to the memory via the chipset; and

the chipset to utilize an Error Correcting Code (ECC) based on an adjacent symbol codeword that is formed in two clock phases and to determine whether an error exists in a plurality of data received by the chipset from the memory, if so, to classify a type of the error based on an H matrix syndrome.

27. The system of claim 26 wherein the memory is a Double Data Rate (DDR) memory.

28. The system of claim 26 wherein the H matrix syndrome is generated by the formula:

$s_{i=} \Sigma\ v_j \times H_{ij}$ for i=0 to 31 and j= 0 to 287.

29. The system of claim 26 wherein the system is a server.